# **Trench Power MOSFET** -20 V, Single P-Channel, SOT-23

### Features

- Leading -20 V Trench for Low R<sub>DS(on)</sub>
- -1.8 V Rated for Low Voltage Gate Drive
- SOT-23 Surface Mount for Small Footprint
- Pb-Free Package is Available

### Applications

- Load/Power Management for Portables
- Load/Power Management for Computing
- Charging Circuits and Battery Protection

Parame	Symbol	Value	Unit		
Drain-to-Source Voltage			V <sub>DSS</sub>	-20	V
Gate-to-Source Voltage			V <sub>GS</sub>	±8.0	V
Continuous Drain	Steady	$T_A = 25^{\circ}C$	I <sub>D</sub>	-2.4	А
Current (Note 1)	State	T <sub>A</sub> = 85°C		-1.7	
	t ≤[]0 s	$T_A = 25^{\circ}C$		-3.2	
Power Dissipation (Note 1)	Steady State	$T_A = 25^{\circ}C$	PD	0.73	W
	t ≤[]0 s			1.25	
Continuous Drain	Steady	$T_A = 25^{\circ}C$	۱ <sub>D</sub>	-1.8	А
Current (Note 2)	State	T <sub>A</sub> = 85°C		-1.3	
Power Dissipation (Note 2)		$T_A = 25^{\circ}C$	PD	0.42	W
Pulsed Drain Current	tp =	[]0 μs	I <sub>DM</sub>	-18	А
ESD Capability (Note 3)	C = 100 pF, RS = 1500 Ω		ESD	225	V
Operating Junction and Storage Temperature			T <sub>J</sub> , T <sub>STG</sub>	–55 to 150	°C
Source Current (Body Diode)			ا <sub>S</sub>	-2.4	А
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			ΤL	260	°C

MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	170	°C/W
Junction-to-Ambient - t < 10 s (Note 1)	$R_{\theta JA}$	100	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	300	

1. Surface-mounted on FR4 board using 1 in sq pad size

(Cu area = 1.127 in sq [1 oz] including traces)

2. Surface-mounted on FR4 board using the minimum recommended pad size.

3. ESD Rating Information: HBM Class 0

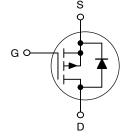


# **ON Semiconductor®**

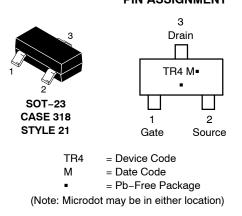
## http://onsemi.com

V <sub>(BR)DSS</sub> R <sub>DS(ON)</sub> TYP		I <sub>D</sub> MAX
–20 V	70 mΩ @ –4.5 V	
	90 mΩ @ –2.5 V	-3.2 A
	112 mΩ @ –1.8 V	





MARKING DIAGRAM & PIN ASSIGNMENT



# **ORDERING INFORMATION**

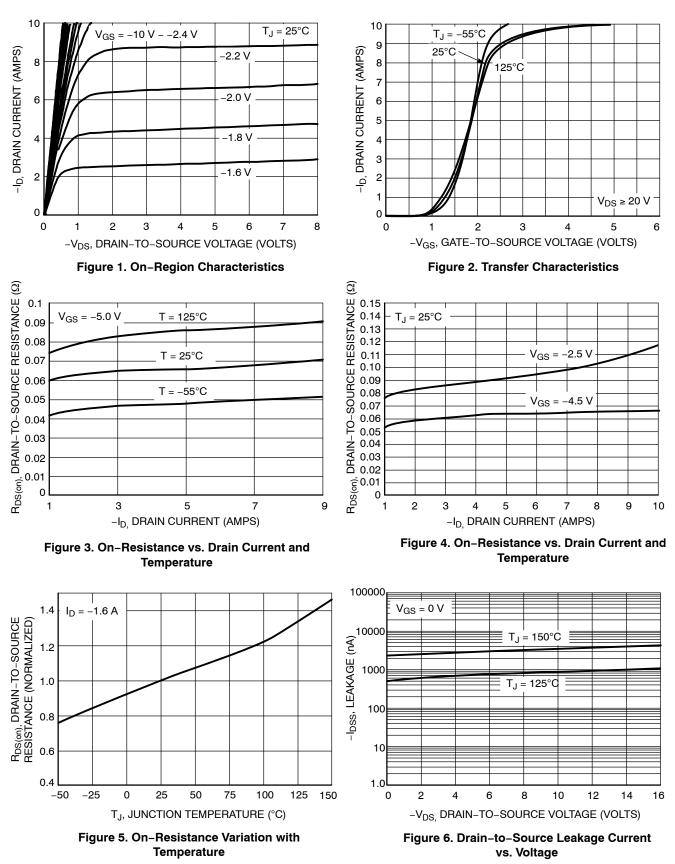
Device	Package	Shipping <sup>†</sup>
NTR4101PT1	SOT-23	3000/Tape & Reel
NTR4101PT1G	SOT-23 Pb-Free	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Characteristic			Min	Тур	Max	Unit
OFF CHARACTERISTICS						•
Drain-to-Source Breakdown Voltage (Note 4) $(V_{GS} = 0 \text{ V}, I_D = -250 \ \mu\text{A})$			-20			V
Zero Gate Voltage Drain Current (Note 4) $(V_{GS} = 0 V, V_{DS} = -16 V)$		I <sub>DSS</sub>			-1.0	μΑ
Gate-to-Source Leakage Current ( $V_{GS} = \pm 8.0 \text{ V}, V_{DS} = 0 \text{ V}$ )		I <sub>GSS</sub>			±100	nA
ON CHARACTERISTICS					•	
Gate Threshold Voltage (Note 4) $(V_{GS} = V_{DS}, I_D = -250 \ \mu\text{A})$		V <sub>GS(th)</sub>	-0.4	-0.72	-1.2	V
Drain-to-Source On-Resistance $(V_{GS} = -4.5 \text{ V}, I_D = -1.6 \text{ A})$ $(V_{GS} = -2.5 \text{ V}, I_D = -1.3 \text{ A})$ $(V_{GS} = -1.8 \text{ V}, I_D = -0.9 \text{ A})$		R <sub>DS(on)</sub>		70 90 112	85 120 210	mΩ
Forward Transconductance ( $V_{DS}$ = -5.0 V, $I_D$ = -2.3 A)				75		S
CHARGES, CAPACITANCES & GA						
Input Capacitance		C <sub>iss</sub>		675		pF
Output Capacitance	(V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = -10 V)	C <sub>oss</sub>		100		
Reverse Transfer Capacitance		C <sub>rss</sub>		75		
Total Gate Charge	$(V_{GS} = -4.5 \text{ V}, V_{DS} = -10 \text{ V}, I_D = -1.6 \text{ A})$	Q <sub>G(tot)</sub>		7.5	8.5	nC
Gate-to-Source Gate Charge	(V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1.6 A)	Q <sub>GS</sub>		1.2		nC
Gate-to-Drain "Miller" Charge	(V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1.6 A)	Q <sub>GD</sub>		2.2		nC
Gate Resistance		R <sub>G</sub>		6.5		Ω
SWITCHING CHARACTERISTICS	(Note 5)					•
Turn-On Delay Time		t <sub>d(on)</sub>		7.5		ns
Rise Time	− (V <sub>GS</sub> = −4.5 V, V <sub>DS</sub> = −10 V,	t <sub>r</sub>		12.6		
Turn-Off Delay Time	$I_{\rm D} = -1.6 \text{ A}, \text{ R}_{\rm G} = 6.0 \Omega$	t <sub>d(off)</sub>		30.2		1
Fall Time		t <sub>f</sub>		21.0		1
DRAIN-SOURCE DIODE CHARAC	TERISTICS					
Forward Diode Voltage	(V <sub>GS</sub> = 0 V, I <sub>S</sub> = -2.4 A)	V <sub>SD</sub>		-0.82	-1.2	V
Reverse Recovery Time		t <sub>rr</sub>		12.8	15	ns
Charge Time	(V <sub>GS</sub> = 0 V, dl <sub>SD</sub> /dt = 100 A/μs, I <sub>S</sub> = −1.6 A)	t <sub>a</sub>		9.9		ns
Discharge Time		t <sub>b</sub>		3.0		ns
Reverse Recovery Charge				1008		nC

Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤ 2%.
Switching characteristics are independent of operating junction temperature.



### TYPICAL PERFORMANCE CURVES (T<sub>J</sub> = 25°C unless otherwise noted)

# **TYPICAL PERFORMANCE CURVES** ( $T_J$ = 25°C unless otherwise noted)

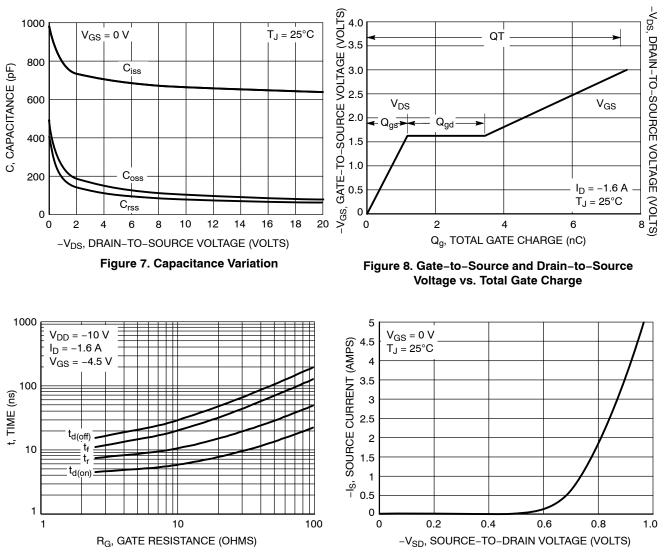
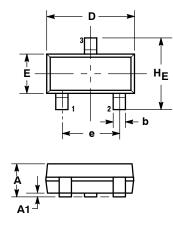


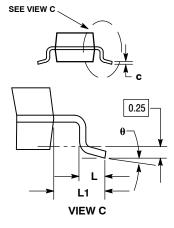
Figure 9. Resistive Switching Time Variation vs. Gate Resistance

Figure 10. Diode Forward Voltage vs. Current

#### PACKAGE DIMENSIONS

SOT-23 (TO-236) CASE 318-08 **ISSUF AN** 





NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

CONTROLLING DIMENSION: INCH. MAXIMUM LEAD THICKNESS INCLUDES 2. 3.

- LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF
- BASE MATERIAL. 4. 318-01 THRU -07 AND -09 OBSOLETE,

NEW STANDARD 318-08.

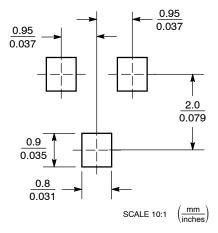
	MILLIMETERS			INCHES			
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
Α	0.89	1.00	1.11	0.035	0.040	0.044	
A1	0.01	0.06	0.10	0.001	0.002	0.004	
b	0.37	0.44	0.50	0.015	0.018	0.020	
с	0.09	0.13	0.18	0.003	0.005	0.007	
D	2.80	2.90	3.04	0.110	0.114	0.120	
E	1.20	1.30	1.40	0.047	0.051	0.055	
е	1.78	1.90	2.04	0.070	0.075	0.081	
L	0.10	0.20	0.30	0.004	0.008	0.012	
L1	0.35	0.54	0.69	0.014	0.021	0.029	
HE	2.10	2.40	2.64	0.083	0.094	0.104	

STYLE 21:

PIN 1. GATE SOURCE

2. 3. DRAIN





\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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